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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,170	02/24/2004	Dae-Whan Back	46158	8281
7590	09/20/2010		EXAMINER	
Peter L. Kendall Roylance, Abrams, Berdo & Goodman, L.L.P. Suite 600 1300 19th Street, N.W. Washington, DC 20036			KAVLESKI, RYAN C	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/784,170	BACK, DAE-WHAN	
	Examiner	Art Unit	
	Ryan C. Kavleski	2475	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 31 August 2010.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-11, 13, 14 and 16 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-11, 13, 14 and 16 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____ .

Response to Amendments

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.
2. The indicated allowability of claims 1,6,13 and 16 is withdrawn in view of the newly discovered reference(s) to Roohparvar et al and prior referenced Witkowski et al. Rejections based on the newly cited references follow.
3. This communication is in response to Applicant's reply filed under 3 CFR 1.111 on 8/31/2010. Claims 1,6,13 and 16 were amended, claims 12 and 15 were canceled, and claims 1-11,13,14 and 16 remain pending.

Amendment to claims 1 and 6 in response to rejection under 35 USC § 112, second paragraph has been considered. The amendment to the claims obviates previously raised rejection, as such this rejection is hereby withdrawn.

Amendment to claims 1 and 6 in response to objection under informalities has been considered. The amendment to the claims obviates previously raised objection, as such this objection is hereby withdrawn.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 4/8/2010 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. **Claims 1-11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsztoo et al (U.S Patent No. 6,639,915 B1)(Tsztoo hereafter) in view of Galdun et al. (US Pat. 5,933,654)(Galdun hereafter) in further view of Witkowski et al (U.S Patent No. 6,201,789 B1)(Wit hereafter) in further view of Schlegel et al. (US Pat. 6,847,677)(Schlegel hereafter).**

Regarding claims 1 and 6, Tsztoo teaches a symbol buffer memory device [refer FIG. 9; 934] of a base station modem [refer FIG. 9; 900], in which the symbol data (i.e., voice data) is stored for transmission to a physical layer [column 13, lines 38-41] comprising: a buffer memory (voice packet buffer memory, refer FIG. 9; 934) for storing the symbol data for the logical channel according to input sequences (i.e., input CHANNEL_ADD, FIG. 9);

a start address table (i.e., channel address memory, refer FIG. 9; 922) for storing address information (the channel address memory stores channel base address values)[column 15 lines 1-10] according to the logical channels (the channel base addresses are based upon CHANNEL# values stored in the content addressable memory (CAM))[column 15 lines 1-10], each of the address information indicating a location of initial symbol data corresponding to each of the logical channels from among the symbol data stored in the buffer memory [column 15, lines 11-19](the CHANNEL# values determine the channel base address within the channel address memory [column 15 lines 1-10], so that voice data can then be read or written to the VPBM according to a channel [column 15 lines 15-55]);

a multiplexer [refer FIG. 9; 930] for selectively outputting the address information stored in the start address table [refer FIG. 9; 922] by an enable signal (i.e. signal sent from request arbiter 928 to mux 930) set for each of the logical channels [column 12, lines 50-54], and

when the symbol data is stored in the buffer (voice data is received from an external source)[column 12 lines 31-38][abstract], the address information indicating positions at which the initial symbol data of each logical channel is stored in the start address table (i.e., channel address memory 922, FIG. 9)(the channel address memory stores channel base address values [column 15 lines 1-10] determined by CHANNEL#'s from the CAM [column 15 lines 1-10], so that voice data can then be read or written to the VPBM according to a channel [column 15 lines 15-55]).

However Tsztoo fails to disclose storing symbol data of the logical channel according to input sequences of the symbol data, so that the symbol data are stored in a continuous arrangement according to a data size of symbol data for the logical channel.

Galdun discloses, in the field of buffer memories, a dynamic buffer memory system in which received data of particular packet sizes (i.e. data size) is stored into a buffer memory area [column 3 lines 17-27], the buffer memory area being fragmented into memory blocks that can be dynamically sized for efficiency so to provide additional memory space for data (i.e. continuous arrangement) [column 5 lines 58-67, column 6 lines 1-10] each fragment referenced by pointers (i.e. head address)[refer Fig. 3][column 6 lines 52-61].

It would have been obvious to one of ordinary skill in the art to given the buffer memory taught by Tsztoo [refer Fig. 4 and 7] for storing voice data in fixed segments according to channel and addressable by base addresses to be modified to incorporate dynamic buffer memory allocation for data of varying sizes as disclosed by Galdun. One would be motivated to do so to provide an efficient management of buffer memory area for data of unknown sizes [refer Galdun; column 1 lines 63-67, column 2 lines 1-7].

However, Tsztoo in view of Galdun fails to disclose that when the symbol data stored in the symbol buffer memory are read and the symbol data of the corresponding channel are separately stored in different sectors, the symbol data stored in the linked sector are continuously read.

Wit teaches a network switch having a plurality of ports for sending and receiving data packets, where it is disclosed that the switch includes a memory having a data packet portions divided into sectors chained together using link addresses. According to the embodiment, the sectors are initially linked into a freepool chain of sectors. As data packets are received, a receive sector chain is created for each network port by pulling sectors from the freepool chain as needed [column 3, lines 54-64][column 33 lines 37-58]. Hence, the link addresses enable the data packets stored in different sectors to be transmitted and received in their entirety using the transmit packet chain for the destination ports for the packets to be sent for transmission (i.e. read continuously)[column 33 lines 51-58].

It would have been obvious to one with ordinary skill in the art at the time of the invention was made to modify the teachings of Tsztoo in view of Galdun to create link information when receiving data for one channel that can be stored in at least two different storage sectors of the buffer memory accordingly, and storing such linking information in the buffer memory and in the start address table to transmit the linked data as taught by Wit. One would be motivated to do so in order to include transmit address links to form transmit packet chain for each port receiving data packets for transmission [refer Wit; column 3, lines 44-47].

However Tsztoo fails to disclose the symbol memory buffer of the base station modem belongs to a mobile communication system, in which the symbol data corresponding to at least one logical channel is coded in at least one encoding ratio (i.e. modulation or encoding scheme) when stored.

Schlegel discloses, in the field of communications, a wireless communications system that communicates data bits (or data symbols, as they are interchangeable) wirelessly over channels by encoding the data using a modulation and encoding scheme [column 4 lines 29-52], the data symbols, or data bits as encoded, can be stored within a buffer memory, which can be designated for before being passed on for transmission [column 12 lines 44-47].

It would have been obvious to one with ordinary skill in the art at the time of the invention was made to modify the teaching of Tsztoo to integrate and implement the symbol memory buffer of the base station modem within a wireless mobile communication system, in which the symbol data corresponding to at least one channel and coded in at least one encoding scheme is stored as taught by Schlegel. One would be motivated to do so to apply a known technique, such as wireless communication, data encoding and storage, to a known device, such as the voice apparatus transmitting voice data over a network taught by Tsztoo, ready for improvement to yield predictable results. Furthermore, one would be motivated to do so to provide a wireless communication system that receives and transmits voice and data information [refer Schlegel; column 6 lines 57-64] that would provide the voice data taught by Tsztoo in an efficient manner through saving processing time and reduction of cost in transmission [refer Schlegel; column 1 lines 55-60].

Regarding claims 2 and 7, Tsztoo teaches when storage of symbols corresponding to a predetermined logical channel has been completed (voice data is stored into the buffer system in a channel by channel basis, with locations in the buffer memory are predetermined for channels)[column 6 lines 42-58], an initial symbol of a channel is subsequently stored at a position of a word in the buffer memory next to the already-stored symbols (the storing of data symbol among channels is continuous in the buffer) [column 10, lines 12-16, 29-32].

Regarding claim 3 and 8, Tsztoo teaches a selection signal input to the multiplexer (i.e., enable signal sent from request arbiter 928 to mux 930) is produced by reading an enable state of a corresponding channel by means of a pulse signal (i.e. control signal, column 14, lines 8-12) of each channel, the enable state of the corresponding channel being stored in the start address table (i.e., channel address memory 922, FIG. 9).

Regarding claims 4-5 and 9-10, Tsztoo fails to disclose that symbol data for one channel are divided and stored in at least two storage sectors of the buffer memory, link information between the storage sectors in which the symbol data for said one channel are stored is stored in the buffer memory and in the start address table.

Wit teaches a network switch having a plurality of ports for sending and receiving data packets. It is disclosed that a switch includes a memory having a data packet portion divided into sectors chained together using link addresses. According to the embodiment, the sectors are initially linked into a freepool chain of sectors. As data

packets are received, a receive sector chain is created for each network port by pulling sectors from the freepool chain as needed [column 3, lines 54-64]. Hence, the link addresses enable the data packets stored in different sectors to be transmitted and received in their entirety.

It would have been obvious to one with ordinary skill in the art at the time of the invention was made to modify the teachings of Tsztoo and Schlegel to create link information when data for one channel are divided and stored in at least two storage sectors of the buffer memory and store such linking information in the buffer memory and in the start address table as taught by Wit. One would be motivated to do so in order to include transmit address links to form transmit packet chain for each port receiving data packets for transmission [refer Wit; column 3, lines 44-47].

Regarding claims 11 and 14, Tsztoo doesn't explicitly disclose that the enable signal represents if the logical channel (i.e. a buffer memory tied to the channel) is operating.

Galdun discloses, in the field of buffer memories, a dynamic buffer memory system in which received data of particular packet sizes (i.e. data size) is stored into a buffer memory area [column 3 lines 17-27], the buffer memory area being fragmented into memory blocks that can be dynamically sized for efficiency so to provide additional memory space for data (i.e. continuous arrangement) [column 5 lines 58-67, column 6 lines 1-10] each fragment referenced by a descriptor that comprises of a status word [refer Fig. 3; 32a-n], a status word received determines a status of particular channels

used with the buffer memory fragments (i.e. representative of operation)[column 4 lines 32-39][column 3 lines 35-44].

It would have been obvious to one of ordinary skill in the art to given the buffer memory taught by Tsztoo [refer Fig. 4 and 7] for storing voice data in fixed segments according to channel and addressable by base addresses to be modified to incorporate dynamic buffer memory allocation for data of varying sizes with a status indicator of the buffer memory for operations as disclosed by Galdun. One would be motivated to do so to provide an efficient management of buffer memory area for data of unknown sizes [refer Galdun; column 1 lines 63-67, column 2 lines 1-7].

3. Claims 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsztoo in view of Galdun in further view of Wit in further view of Schlegal , as applied to claims 1 and 6 above, in further view of Roohparvar et al. (U.S Patent No. 6,851,026)(Rooh hereafter).

Regarding claims 13 and 16, Tsztoo teaches that the buffer memory comprises a first memory and a second memory.

However, Tsztoo doesn't explicitly disclose that the symbol data of each channel corresponding to a first frame is first recorded in the first memory, and all symbol data corresponding to a second frame inputted next to the first frame are recorded in the second memory so that the symbol data stored in the first memory is read

simultaneously when the symbol data of the next input frame is stored in the second memory.

Rooh discloses, in the field of data buffer memory, a memory that is organized into a plurality of independent banks (i.e. sectors) that allow read access to be performed simultaneously with a write operation to any other bank [column 6 lines 21-35][abstract].

It would have been obvious to one of ordinary skill in the art given the teachings of Tsztoo for storing data into various sectors within a buffer memory in accordance to channels to be modified to latch write and read operations of a memory storing data communications so that data can be read from one data location while data is being written to another data location as taught by Rooh, so that data already received and stored in a buffer sector taught by Tsztoo can be read while incoming data is concurrently being stored in a separate buffer sector. One would be motivated to do so to provide continuous data communications when data is being read and written concurrently into memory [refer Rooh; abstract].

Response to Arguments

4. Applicant's arguments, see page 6, filed 8/31/2010, with respect to the consideration of IDS filed 4/8/2010 have been fully considered and are persuasive. The IDS and its contents have been considered.

5. Applicant's arguments, see page 7, filed 8/31/2010, with respect to the allowability of claims 12 and 15, which have been incorporated into claims 1 and 6 respectively, have been fully considered. However, upon a further consideration, a new grounds of rejection has been made in view of previously cited prior art Witkowski and newly discovered prior art Roohparvar. Prosecution has accordingly been reopened.

1. Regarding claims 1 and 6, the limitations " when the symbol data stored in the symbol buffer memory are read and the symbol data of the corresponding channel are separately stored in different sectors, the symbol data stored in the linked sector are continuously read" was previously indicated as allowable subject matter.

In further consideration of the prior art with regards to Witkowski et al, the indicated allowable subject matter has been withdrawn because Witkowski discloses that a memory having a data packet portions divided into sectors chained together using link addresses. Witkowski discloses that the sectors are initially linked into a freepool chain of sectors, as data packets are received, a receive sector chain is created for each network port by pulling sectors from the freepool chain as needed, allowing the sectors to be linked together [column 3, lines 54-64][column 33 lines 37-58]. Hence, the link addresses enable the data packets stored in different sectors to be transmitted and received in their entirety using the transmit packet chain for the destination ports for the packets to be sent for transmission, which meets the criteria of being read continuously [column 33 lines 51-58].

Accordingly, examiner asserts based upon this disclosure that it would have been obvious to one with ordinary skill in the art at the time of the invention was made to modify the teachings of Tsztoo in view of Galdun to create link information when receiving data for one channel that can be stored in at least two different storage sectors of the buffer memory accordingly, and storing such linking information in the buffer memory and in the start address table to transmit the linked data as taught by Wit. One would be motivated to do so in order to include transmit address links to form transmit packet chain for each port receiving data packets for transmission [refer Wit; column 3, lines 44-47].

Furthermore, claims 13 and 16 have been reconsidered and rejected over the newly discovered prior art, Roohparvar et al as indicated in the above rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan C. Kavleski whose telephone number is 571-270-3619 and fax number is 571-270-4619. The examiner can normally be reached on Mon-Fri 7:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dang T. Ton can be reached on 571-272-3171. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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